WHAT IS CLAIMED IS:

1. A television signal receiver, comprising:

a first circuit board including a memory and control circuitry for controlling an operation of the receiver, the control circuitry controlling the operation of the receiver in response to data stored in the memory; and

a second circuit board operably coupled to the first circuit board via IIC bus lines, the second circuit board including a controller, coupled to the IIC bus lines, for generating first control signals in accordance with a first signal format in a first operational state and second control signals in accordance with a second signal format in a second operational state,

the controller placing the memory into an unpowered state during the second operational state, the memory being coupled to means for preventing the memory from keeping the control lines at a low state when the memory is in the unpowered state,

wherein the memory and the control circuitry are coupled to the IIC bus lines, and the controller transmits the first control signals to the memory via the IIC bus lines without affecting the control circuitry in the first operational state, and transmits the second control signals to the control circuitry via the control lines without affecting the memory in the second operational state.

2. The television signal receiver according to claim 1, further comprising means for preventing the memory from keeping the control lines in the low state while the memory is in the unpowered state comprises a zener diode.

3. The television signal receiver according to claim 1, wherein the memory includes operational data for controlling deflection circuitry and the control circuitry controls the deflection circuitry in response to the operational data.

4. The television signal receiver according to claim 3, wherein the first operational state corresponds to an OFF state of the receiver, and the second operational state corresponds to an ON state of the receiver.

5. The television signal receiver according to claim 3, wherein the first control signal corresponds to IIC compliant signals and the second control signals are PWM signals.

6. The television signal receiver according to claim 3, wherein the control circuitry is coupled to the IIC bus lines via bipolar transistors.

7. A signal processing apparatus, comprising:

a first circuit board including first electronic circuitry, and second electronic circuitry for controlling at least one operation of the receiver; and

a second circuit board operably coupled to the first circuit board via control lines, the second circuit board including a controller, coupled to the control lines, for generating first control signals in accordance with a first signal format in a first operational state and second control signals in accordance with a second signal format in a second operational state,

the second electronic circuitry being placed in an unpowered state during the second operational state, the second electronic circuitry being coupled to means for preventing the first electronic circuitry from keeping the control lines at a low state when the second electronic circuitry is in the unpowered state, and

the first and second electronic circuitry are coupled to the control lines, and the controller transmits the first control signals to the first electronic circuitry via the control lines without affecting the second electronic circuitry in the first operational state, and transmits the second control signals to the second electronic circuitry via the control lines without affecting the first electronic circuitry in the second operational state.

8. The signal processing apparatus of claim 7, wherein the first electronic circuitry comprises a memory circuit having operational data stored therein for controlling the second electronic circuitry, the controller retrieving the operational data in the first operational state and controlling the second electronic circuitry in response to the operational data in the second operational state.

9. The signal processing apparatus of claim 8, wherein the operational data comprises voltage data for controlling deflection circuitry, and the second electronic circuitry controls the deflection circuitry in response to the voltage data.

10. The signal processing apparatus of claim 9, wherein the first operational state corresponds to the apparatus being in an OFF state and the controller and the first electronic circuitry is powered by a standby power supply, and the second operational state corresponds to the apparatus being in the ON state.

11. The signal processing apparatus of claim 7, further comprising means for preventing the first electronic means from keeping the control lines at a low level during an unpowered state of the first electronic circuitry.

12. The signal processing apparatus of claim 7, wherein the first control signals comply with the IIC standard and the second control signals comprise pulse width modulated signals.

13. A method of operating a television signal receiver, the method comprising steps of:

providing first and second circuit boards coupled via control lines, the first circuit board having a memory device and control circuitry included thereon and coupled to the control lines, the second circuit board having a controller included thereon and coupled to the control lines;

transmitting via the control lines, first control signals in accordance with a first signal format from the controller on the second circuit board to the memory device

on the first circuit board, without affecting the control circuitry, when the receiver is in a first operational state; and

transmitting via the control lines, second control signals in accordance with a second signal format from the controller to the control circuitry on the first circuit board, without affecting the memory device, when the receiver is in a second operational state; and

placing the memory device in an unpowered state during the step of transmitting the second control signals, the memory device being coupled to means for preventing the memory device from keeping the control lines in a low state when the memory device is placed in the unpowered state.

14. The method of claim 14, wherein the first operational state corresponds to the receiver being in the OFF state wherein the controller and the memory is supplied by a standby power supply, and the second operational state corresponds to the receiver being in an ON state.

15. The method of claim 15, wherein the first control signals enable the controller to read data from the memory.

16. The method of claim 16, further comprising the step of controlling deflection circuitry via the control circuitry in response to data read from the memory.

17. The method of claim 14, wherein the first transmitting step comprises transmitting the first control signals in accordance with the IIC standard.

18. The method of claim 14, wherein the second transmitting step comprises transmitting the second control signals as PWM signals.

19. The method of claim 14, wherein the providing step comprises providing the first circuit board having the control circuit coupled to the control lines via bipolar transistors.